

Model Name: GA-H81M-D3V-JP JP

SHEET

TITLE

Revision 1.01

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS X1 *3 SLOT
16	PCI SLOT (NA)
17	ITE 8620 LPC IO
18	COM,KB_MS_USB,USB30_20
19	HWM,FAN CTRL,OV
20	DUAL BIOS
21	FP,FUSB,SPK,SATALED
22	Realtek ALC887-VD2
23	REAR AUDIO JACK
24	REALTEK RTL8111F
25	DISCRETE POWER
26	ATX
27	VCORE ISL95812_1

28	VCORE ISL95812_2
29	RT8120_DDR POWER
30	LPT
31	DVI
32	IT8892E (NA)
33	USB3 VL805

Gigabyte Technology

Cover Sheet

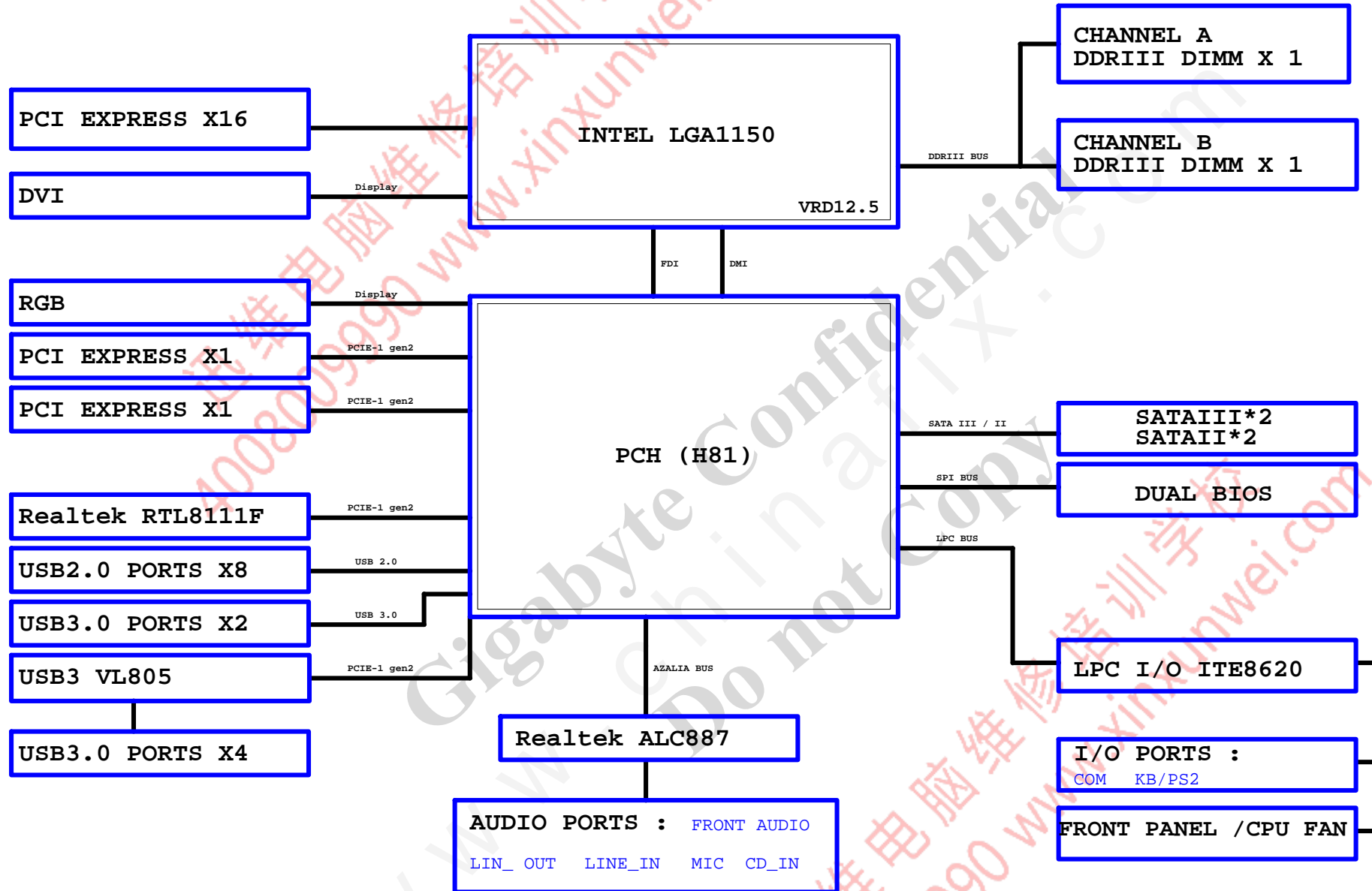
Size	Document Number	GA-H81M-D3V-JP JP	Rev
Custom			1.01
Date:	Friday, November 08, 2013	Sheet	1 of 33

Circuit or PCB layout change

2013/05/17

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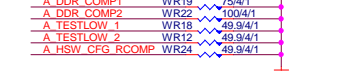
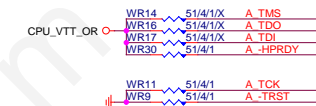
BLOCK DIAGRAM



CPU PU/PD



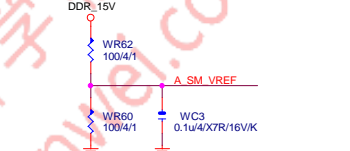
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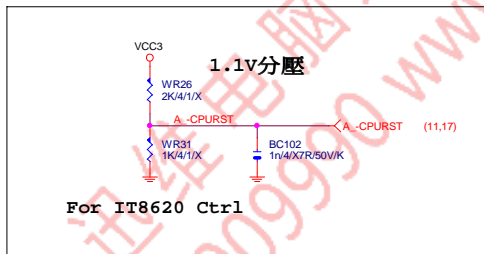
SM REF



A circuit diagram showing a voltage source V_1 in series with a resistor R_1 , connected to a load resistor R_L . The current flowing through the circuit is labeled i .



-CPURST



FDI:12/4/5/4/12(breakout min 6/4/4/4/6)
Impedance=85 +/- 17.5%

FDI_TXP[0..1] >> FDI_TXP[0..1] (9)

FDI_TXN[0..1] >> FDI_TXN[0..1] (9)

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CPU LGA1150-A

GA-H81M-D3V-JP JP

Rev	1.0
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LGA1150

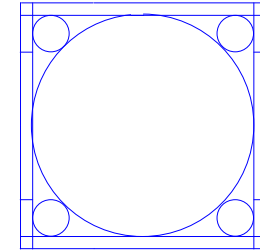
(A)

LGA1150

(B)

LGA1150

(CR)

CR
CPU RETAINTION/X

LGA1150



ILM_BP/1156/CSP/ILM_BP/1156/CSP/[12KRC-0F0001-52R_12KRC-0F0001-51R]

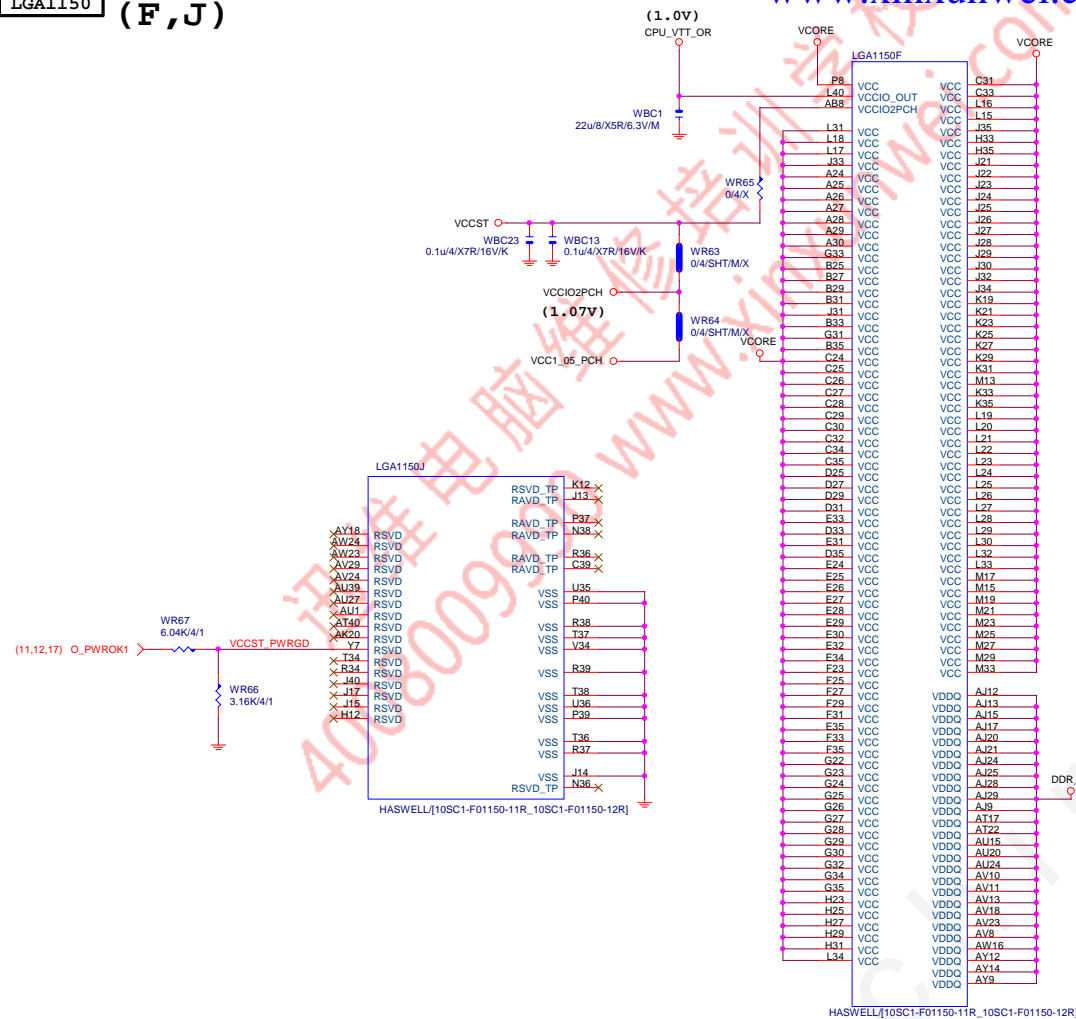
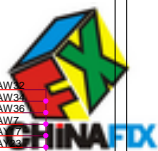
DDR BUS

LGA1150A		LGA1150B	
MAAA0	AU13	MAAB0	AL19
MAAA1	AV16	MAAB1	AK23
MAAA2	AU16	MAAB2	AM22
MAAA3	AW17	MAAB3	AM23
MAAA4	AU17	MAAB4	AP23
MAAA5	AW18	MAAB5	AL23
MAAA6	AW17	MAAB6	AY24
MAAA7	AT18	MAAB7	AV25
MAAA8	AU18	MAAB8	AU26
MAAA9	AT19	MAAB9	AW25
MAAA10	AW11	MAAB10	AP18
MAAA11	AV19	MAAB11	AK38
MAAA12	AU19	MAAB12	AV26
MAAA13	AY10	MAAB13	AR15
MAAA14	AT20	MAAB14	AV27
MAAA15	AU21	MAAB15	AV28
MODT_A0	AW10	MODT_B0	AM17
MODT_A1	AY8	MODT_B1	AL16
AW9		AM16	
AW8		AK15	
AW33		AM26	
AW33		AM25	
AU31		AP25	
AT31		AP26	
AU33		AL26	
AT33		AL25	
AU33		AR26	
AT31		AL23	
AW31		AR26	
SBAA0	SBAA0	SBAB0	AK17
SBAA1	SBAA1	SBAB1	AL18
SBAA2	SBAA2	SBAB2	AW28
CKEA0	CKEA0	CKEB0	AW29
CKEA1	CKEA1	CKEB1	AW29
CSA0	CSA0	CSB0	AP17
CSA1	CSA1	CSB1	AM15
DCLKA0	DCLKA0	DCLKB0	AM20
DCLKA1	DCLKA1	DCLKB1	AP22
DCLKA2	DCLKA2	DCLKB2	AP21
DCLKA3	DCLKA3	DCLKB3	AP21
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LGA1150 (F,J)

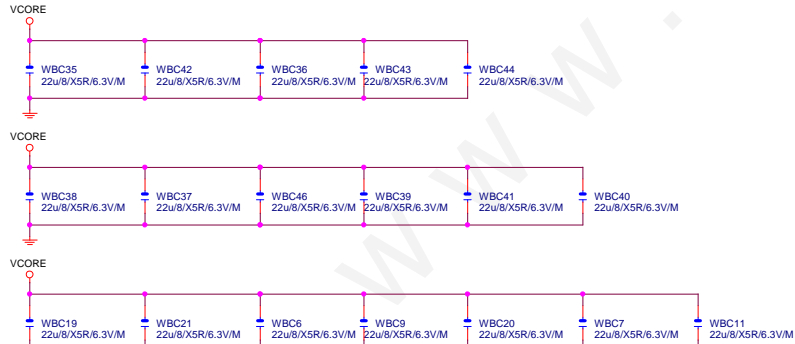
www.xinxunwei.com 400-800-9990

LGA1155 (G,H,I)



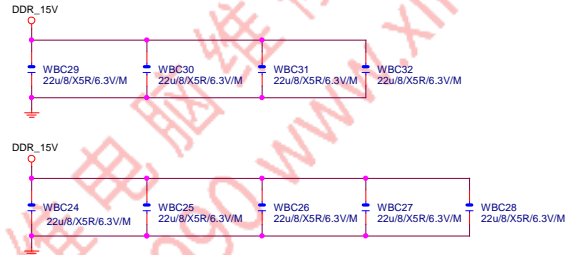
VCore CAP

(X18)



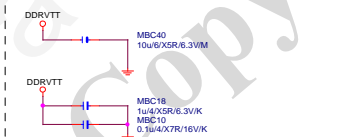
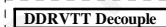
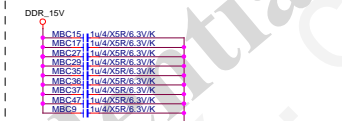
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(X9)



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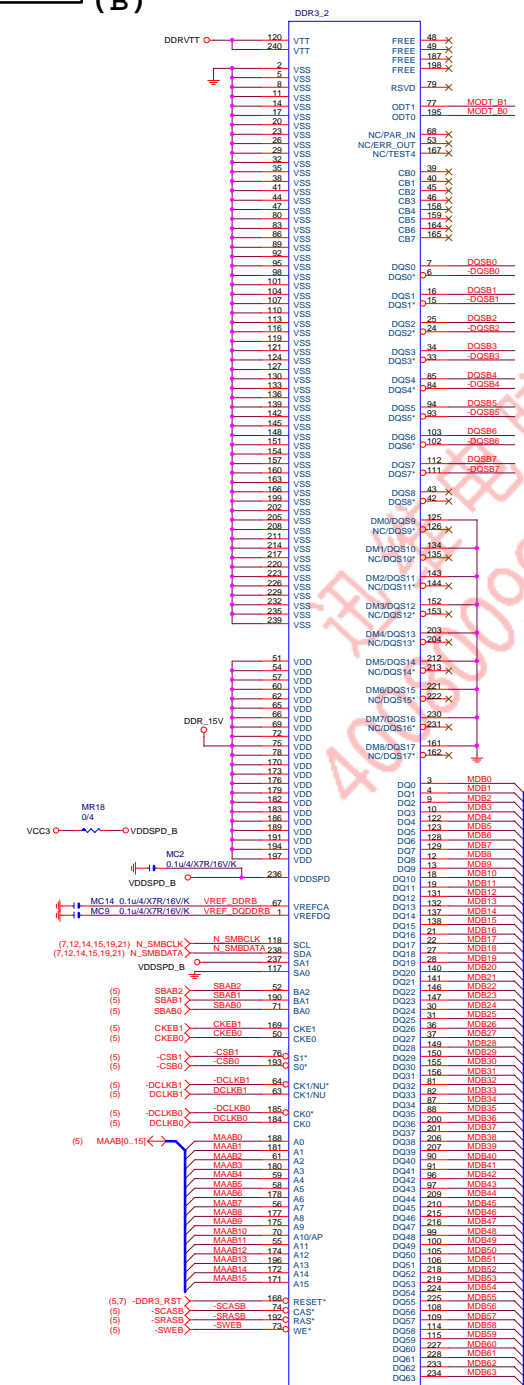
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CPU LGA1150-C				
Size	Document Number			Rev
Custom	GA-H81M-D3V-JP JP			1.01
Date:	Friday, November 08, 2013		Sheet	6 of 33





DDR3

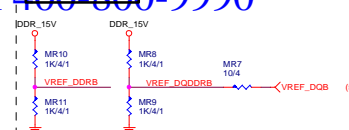
(B)



DDR3/240/BK/VA/D
BLACK CONNECTOR



DDR3 VREF



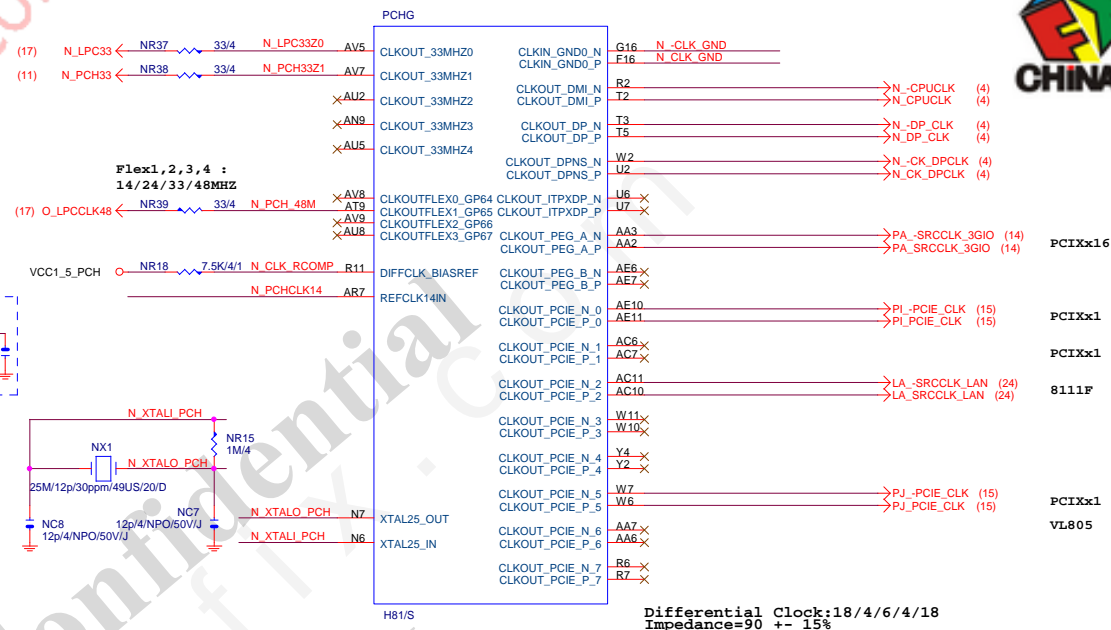
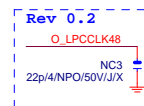
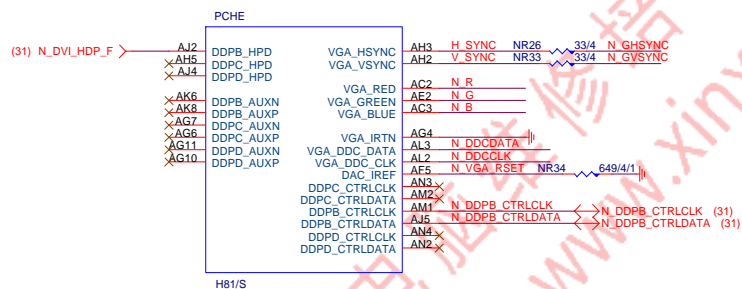
COUPON



CPU

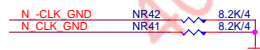


Gigabyte Technology		
Title		
DDRIII CHANNEL B		
Size		
Document Number		
GA-H81M-D3V-JP JP		
Rev		
1.01		
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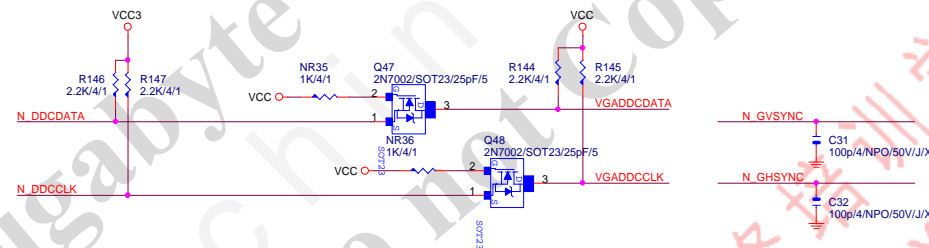


Differential Clock:18/4/6/4/18
Impedance=90 +- 15%

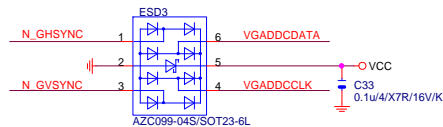
VGA DDC



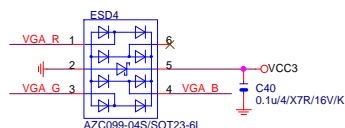
Mount for integrated clock Generation
Mode



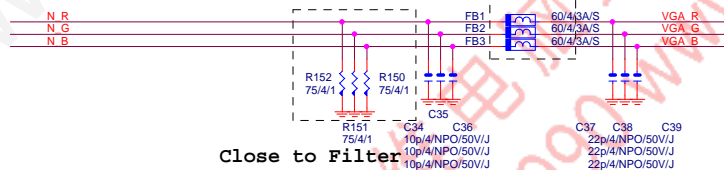
VGA DDC



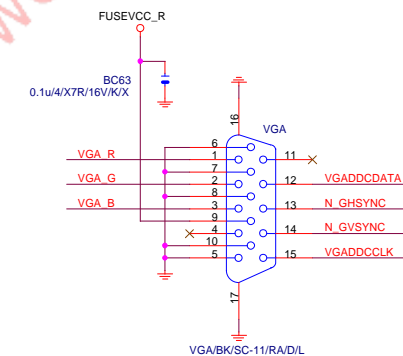
SSOP6 ESD



AZC099-04S/SOT23-6L



Close to Filter



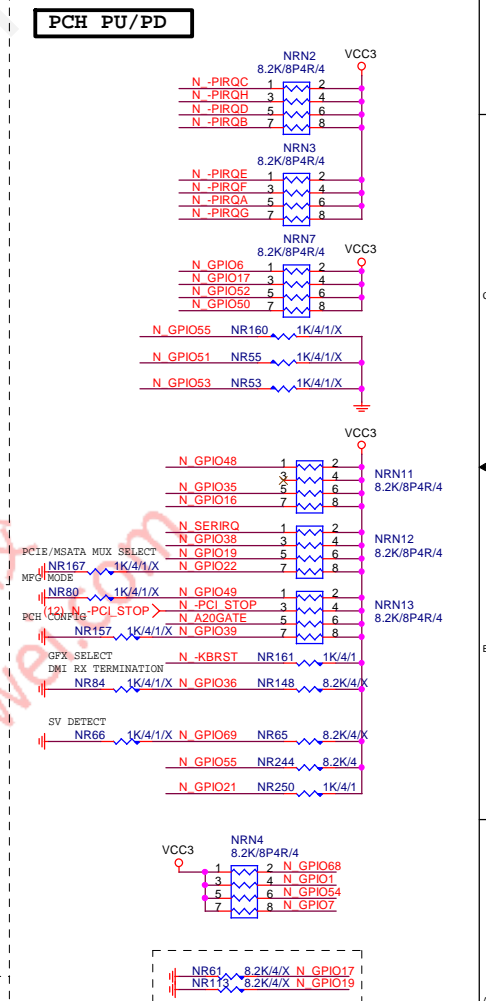
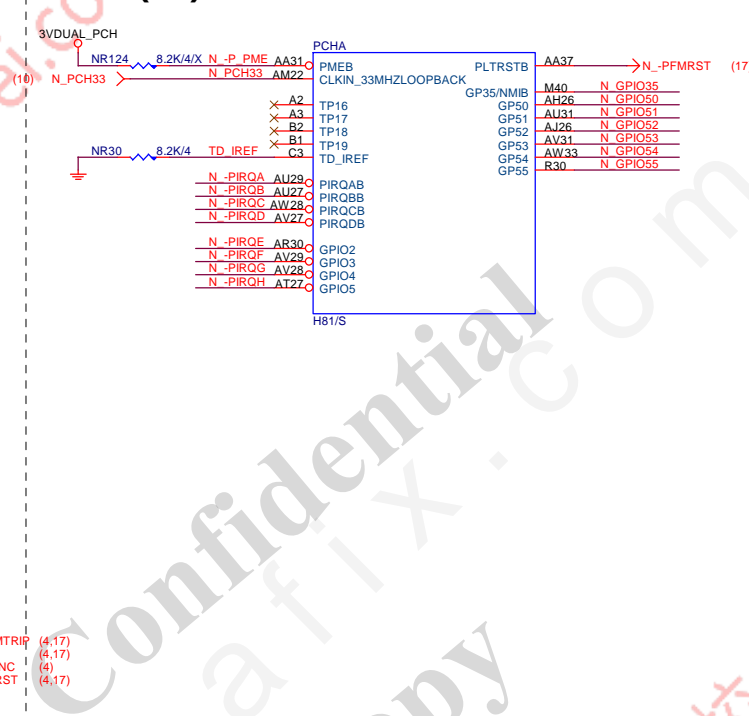
BLACK CONNECTOR

Gigabyte Technology

PCH DISPLAY ,CLK BUFFER

GA-H81M-D3V-JP JP

Rev
1.01

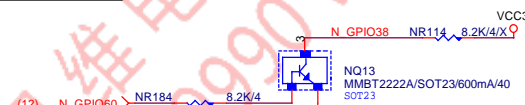


N SATA5TXP NC57 0.01u4/X7R/25V/K N SATA5TXPC
 N SATA5TXN NC56 0.01u4/X7R/25V/K N SATA5TXNC
 N SATA5RXN NC55 0.01u4/X7R/25V/K N SATA5RXNC
 N SATA5RXP NC54 0.01u4/X7R/25V/K N SATA5RXPC

SATA2_3
 SATA27/BK/H/OP/VA/D/1/B
BLACK CONNECTOR

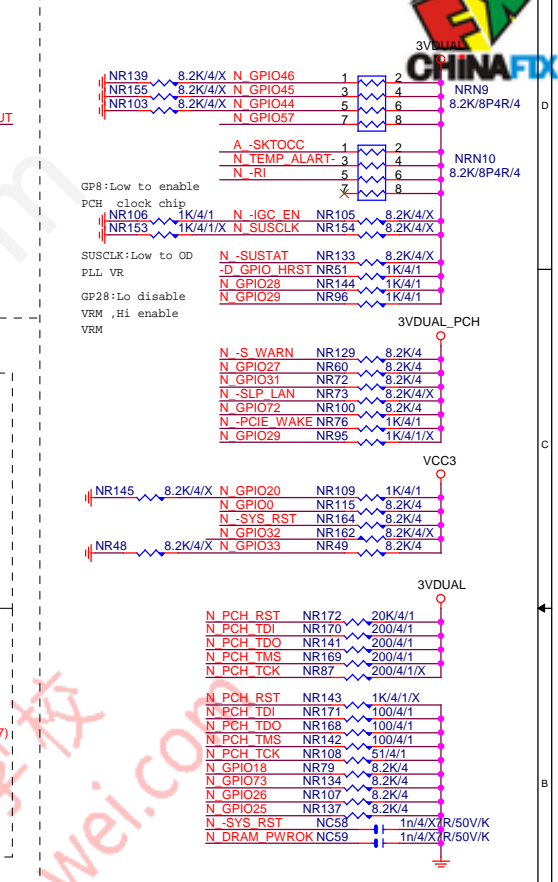
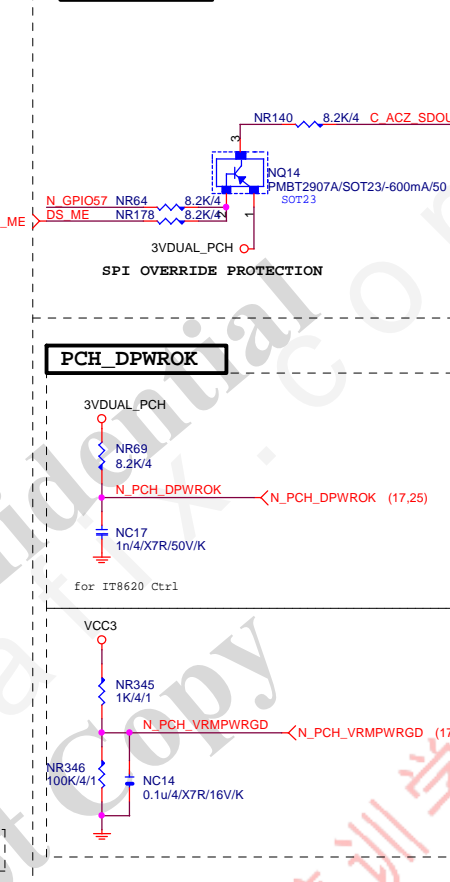
GPI037 PU VCC3 ENABLE SBA
For H87&B85

GPI038 Ctrl



ACZ_SDOUT

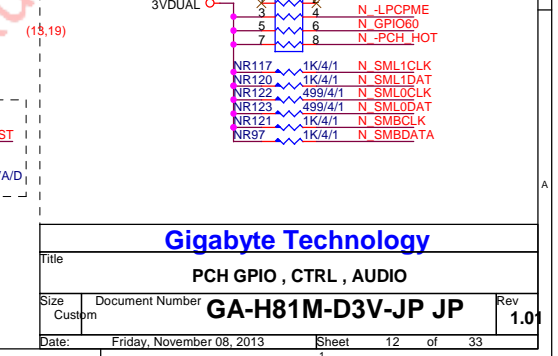
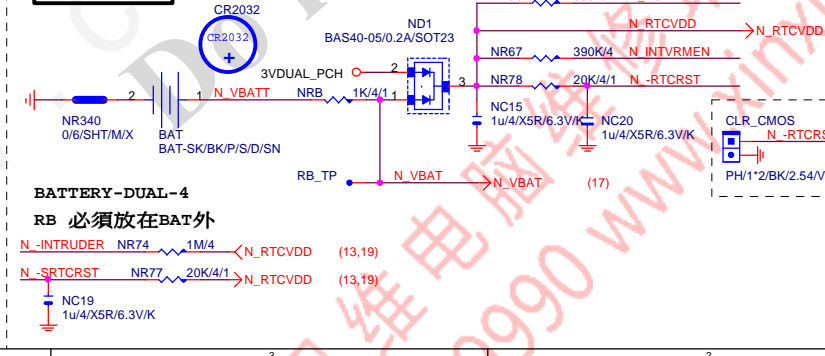
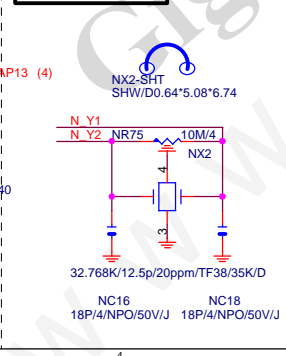
PCH	PU/PD
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HSW_STRAP13

32.768KHZ

CLR_CMOS



Gigabyte Technology

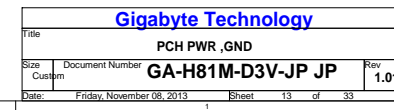
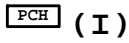
PCH GPIO , CTRL , AUDIO

GA-H81M-D3V-JP JP

1.01

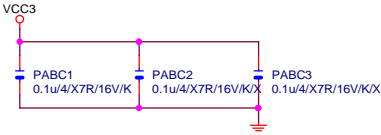
Date:	Friday, November 08, 2013	Sheet	12	of	33
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SHT PWR

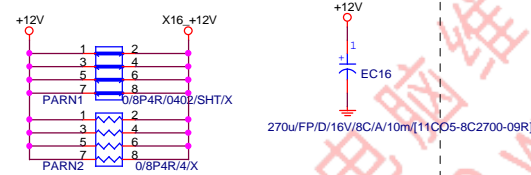




PCIEX16 CAP



PCIEX16 PROTECT SHT



PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

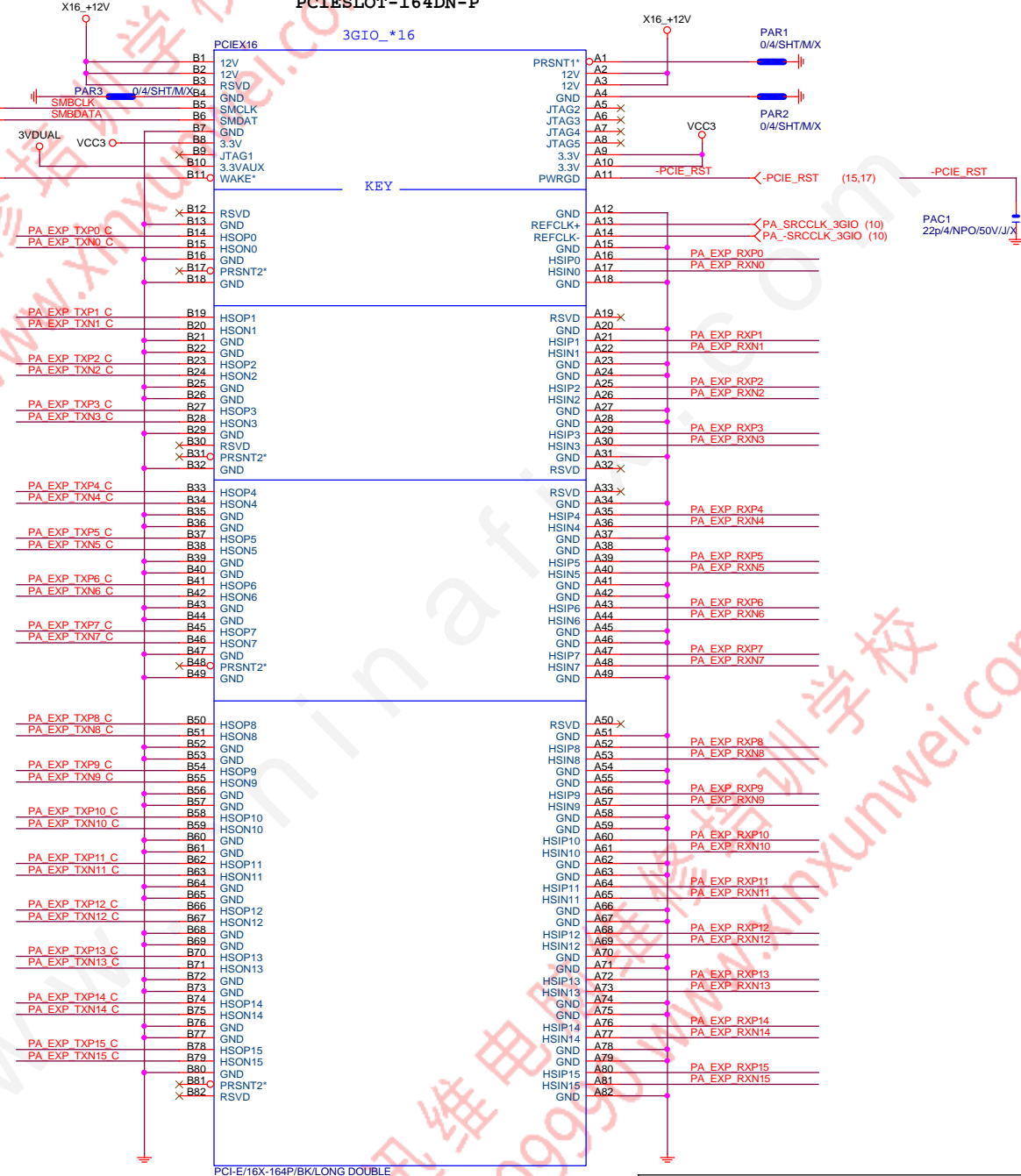
PA EXP RXIP0.15] >>> PA_EXP_RXIP[0.15] (4)
PA EXP RXN0.15] >>> PA_EXP_RXN[0.15] (4)
PA EXP TXIP0.15] >>> PA_EXP_TXIP[0.15] (4)
PA EXP TXN0.15] >>> PA_EXP_TXN[0.15] (4)

The auxiliary reset circuit is only required for PCIe Gen3 margining and functional link training

PCIEX16 SLOT

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PCIESLOT-164DN-P

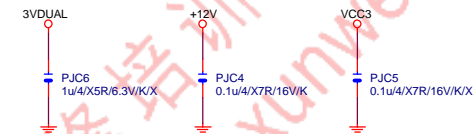
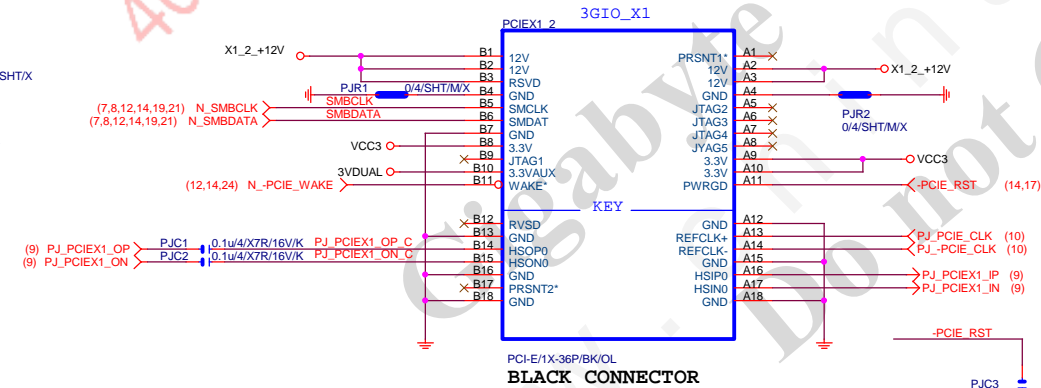
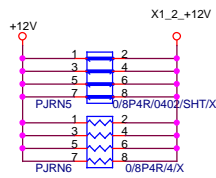
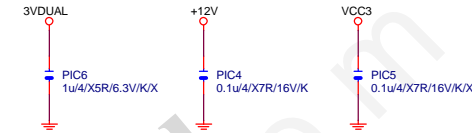
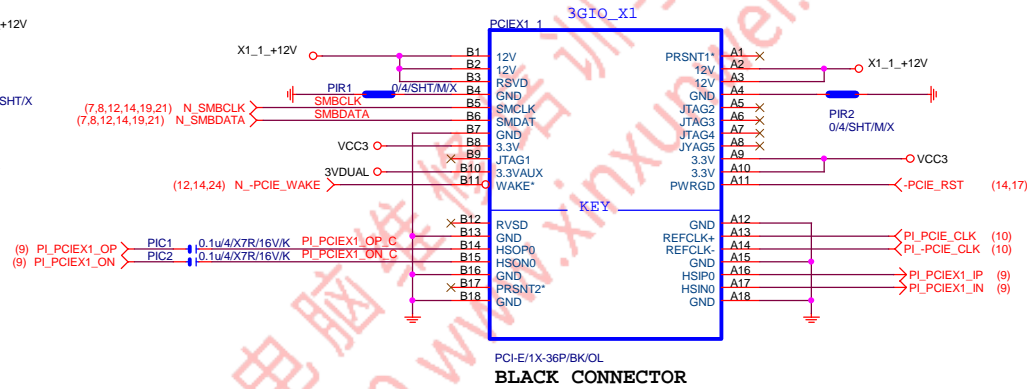
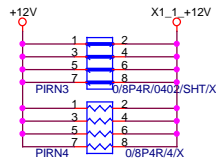


BLACK CONNECTOR

Gigabyte Technology

Title			PCI EXPRESS * 16	
Size			GA-H81M-D3V-JP JP	
Custom			Rev 1.01	
Date:			Friday, November 08, 2013	Sheet 14 of 33

PCIEX1 SLOT



Gigabyte Technology

Title		
PCI EXPRESS X 1 PORT		
Size	Document Number	Rev
Custom	GA-H81M-D3V-JP JP	1.01
Date:	Friday, November 08, 2013	Sheet 15 of 33



Gigabyte Technology		
Title		
PCI SLOT 1&2		
Size	Document Number	Rev
Custom	GA-H81M-D3V-JP JP	1.01
Date	Friday, November 08, 2013	Sheet 16 of 33
	2	1



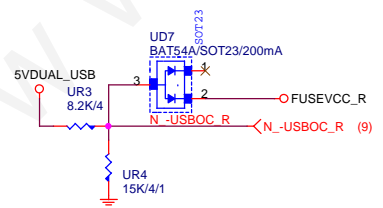
COM

COM RI

USB30_20

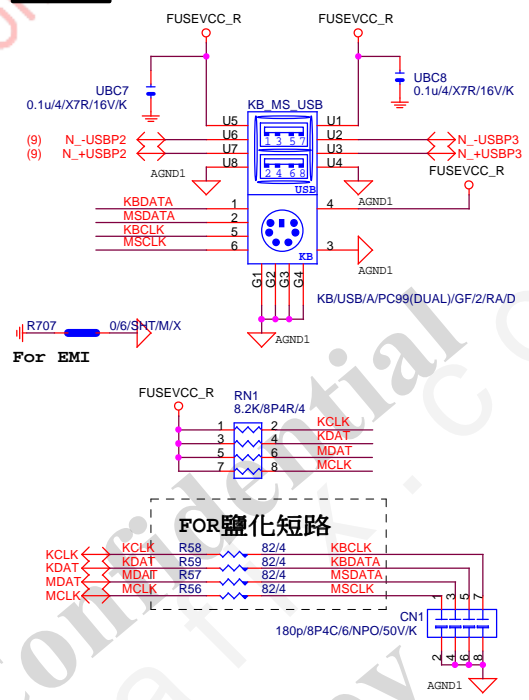
USB30_20 PWR

-USBOC_R



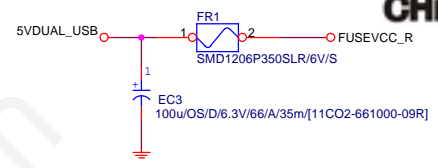
www.xinxunwei.com 400-800-9990

KB/MS



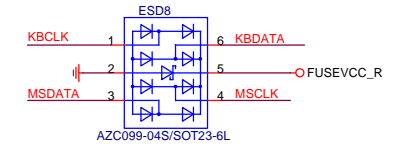
USB2.0 PWR

FUSE-0805
KB_MS_USB 2-Port 2.0A

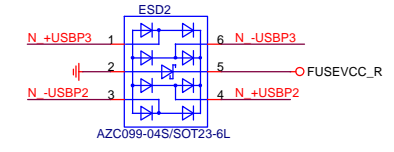


Close to connector

KB/MS ESD



USB2.0 ESD

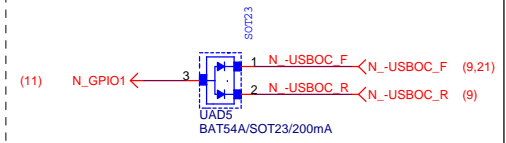


USB30_20 ESD PROTECT

USB3.0 ESD

USB2.0 ESD

USB POWER PROTECT

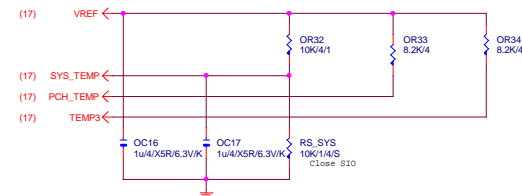


Gigabyte Technology

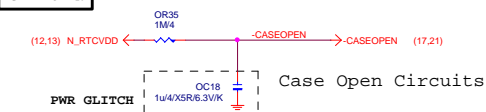
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Size	Custom	Document Number	GA-H81M-D3V-JP JP		Rev 1.01
Date:	Friday, November 08, 2013		Sheet	18 of 33	



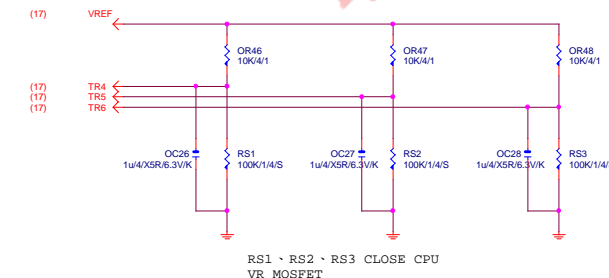
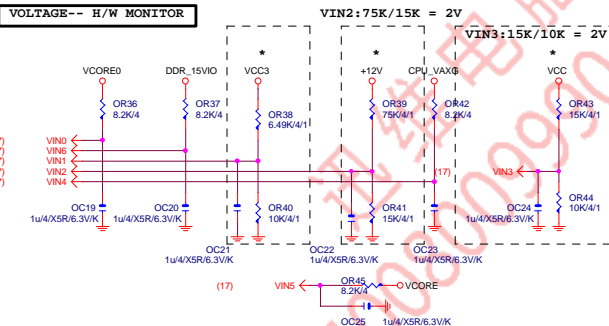
TEMP H/W MONITOR



CASE OPEN

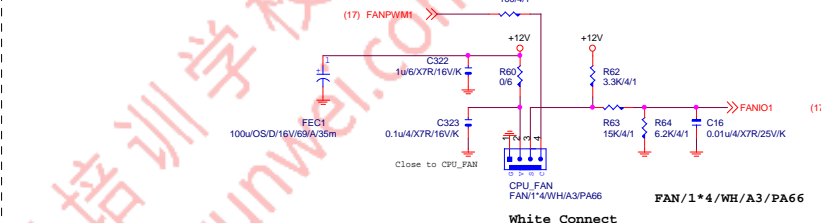


VOLTAGE-- H/W MONITOR

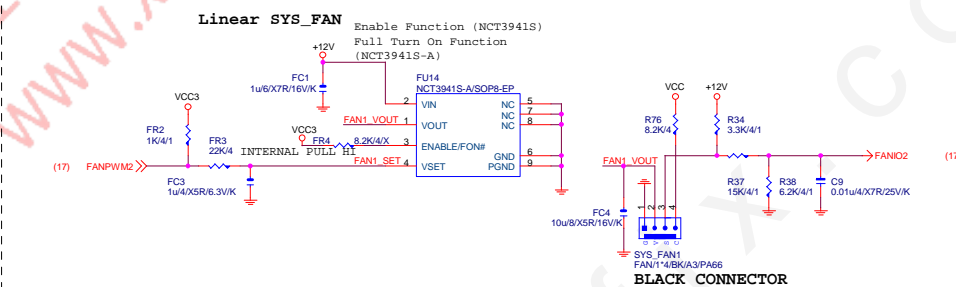


RS1、RS2、RS3 CLOSE CPU VR MOSFET

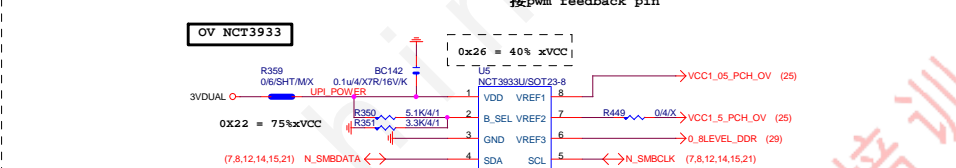
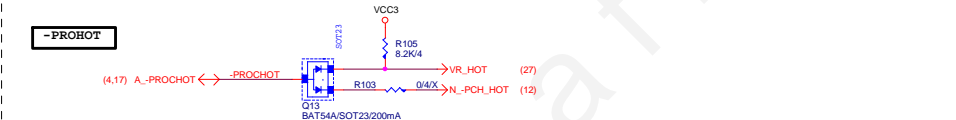
CPU SMART FAN



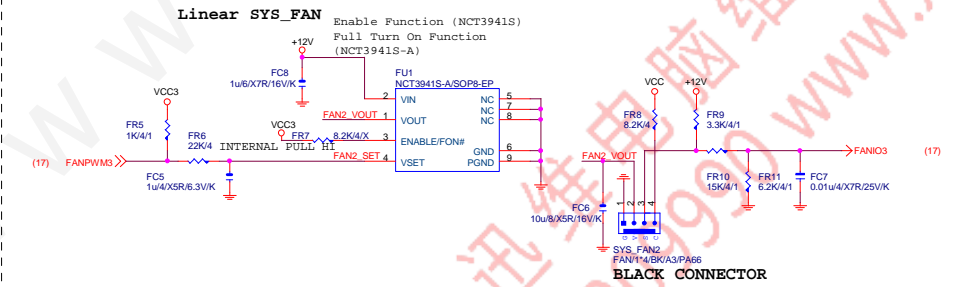
SYS SMART FAN

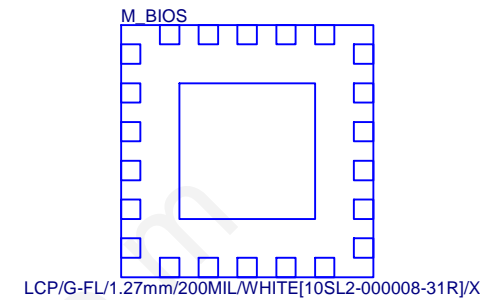
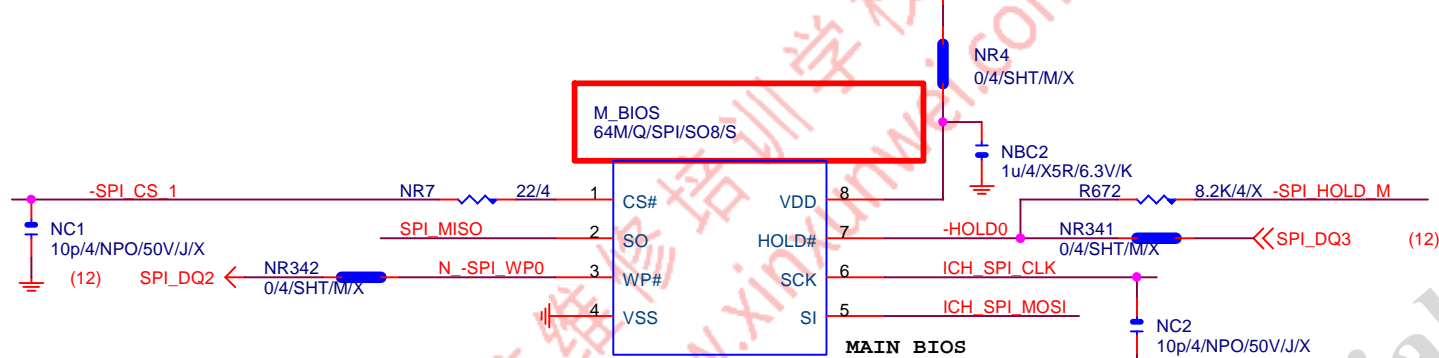


-PROHOT



NCT3933	0X2A	0X20	0X22
VREF1	DDRVT	VREF_DDRA_DQ	PCH Core
VREF2	VREF_DDRA_CA	N/A	VCC1_5_PCH
VREF3	VREF_DDRA_CA	VREF_DDRB_DQ	SMREF

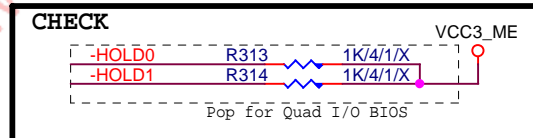
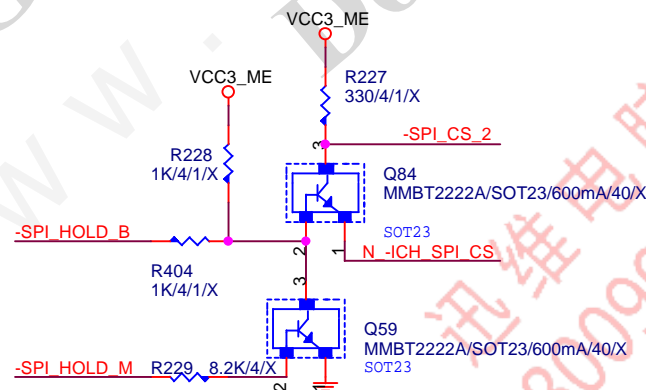
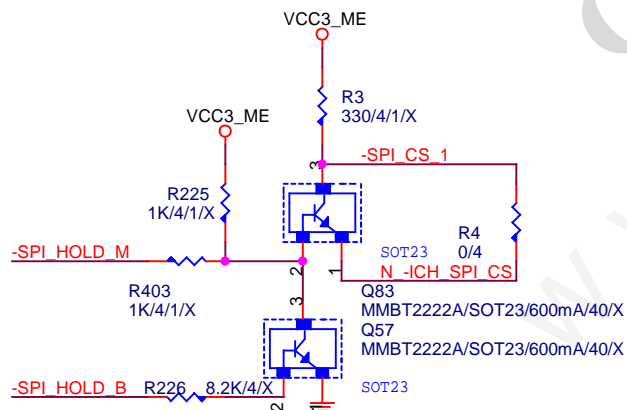
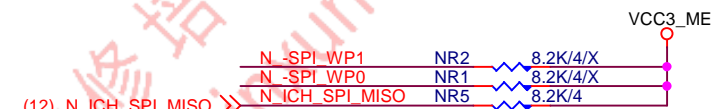




BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

1 means floating
0 means PD 1K

MOSI For DMI RX Termination Voltage



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DUAL BIOS

Title	GA-H81M-D3V-JP JP		
Size Custom	Document Number	Rev	1.01
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F_USB30

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F_USB30_PWR

SATA_PWR

-USB0C_F

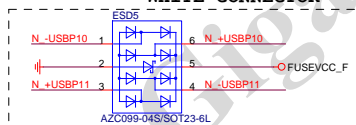
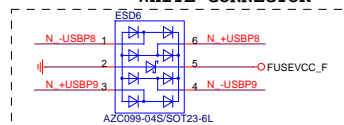
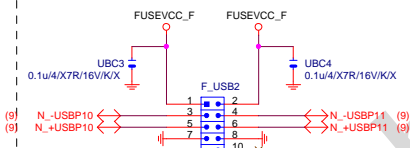
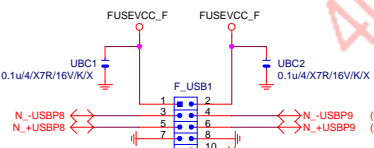
F_USB30 ESD PROTECT

SPKR

FRONT USB1

FRONT USB2

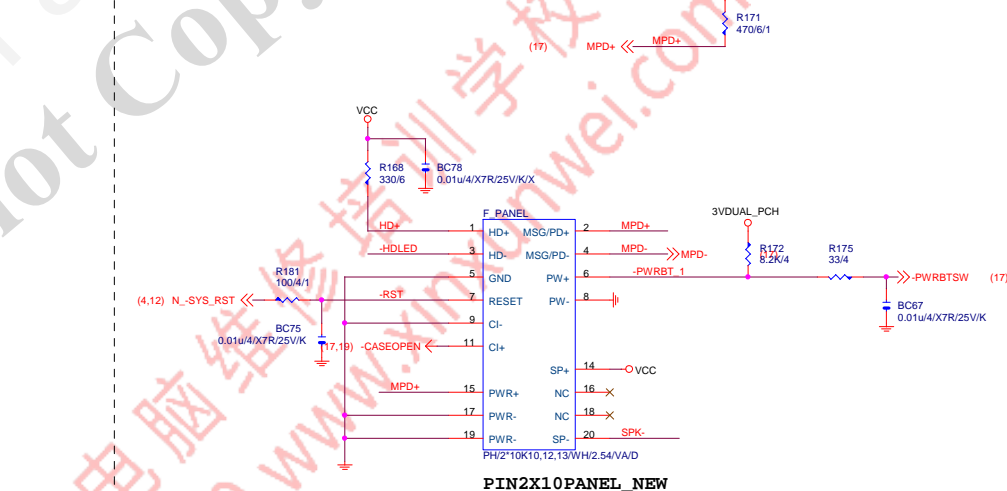
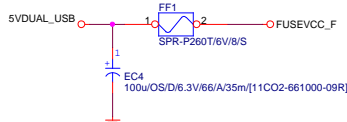
INTEL FRONT PANEL



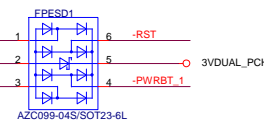
Close to connector

Close to connector

FUSE-0805
F_USB1, F_USB2 4-Port 2.6A



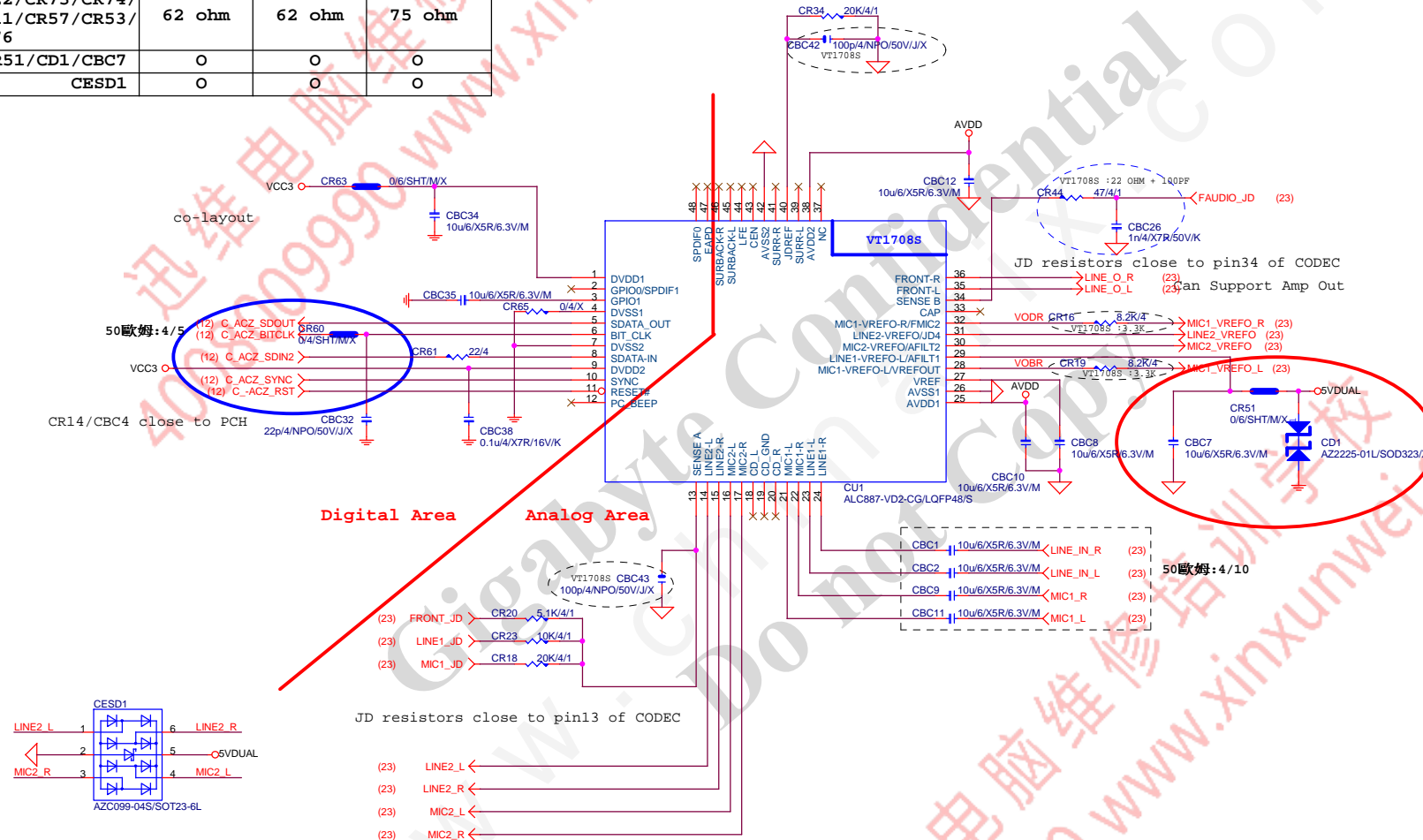
PIN2X10PANEL_NEW



Gigabyte Technology			
FP,F_USB,USB PWR,SPKR,SATA LED			
GA-H81M-D3V-JP JP			
Size	Custom	Rev	1.01
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AZALIA CODEC **ALC892/ALC887-VD2/VT1708-CE Colay**

	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	O	O	O

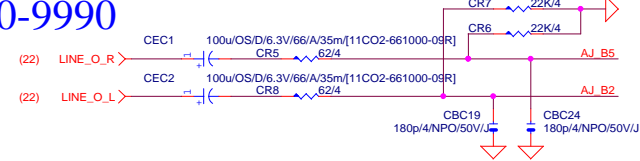


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Title	HD AUDIO ALC887B-VD2/VT1708S/VT2021		
Size	Document Number	GA-H81M-D3V-JP JP	Rev 1.01
Custom			
Date:	Friday, November 08, 2013	Sheet 22 of 33	1

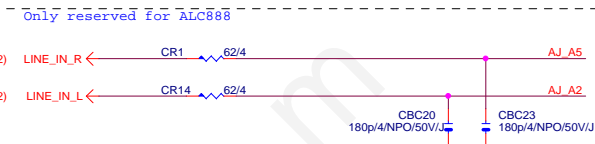


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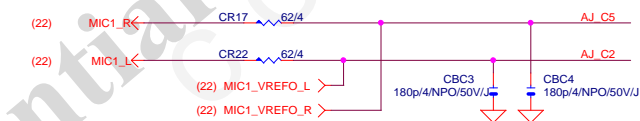


LINE-IN

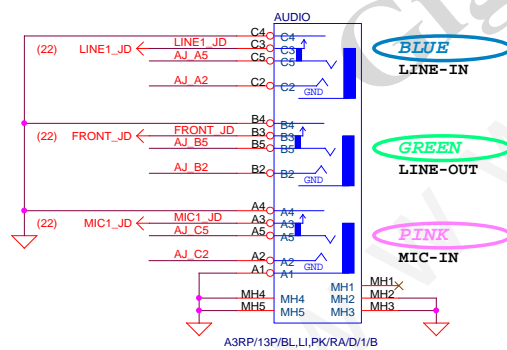
Verify MIC function
in LINE-in



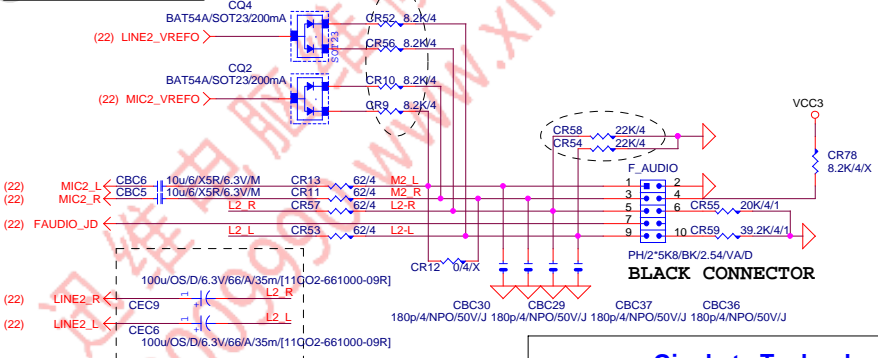
MIC-IN



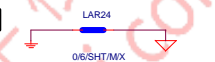
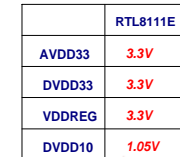
SPDIF_OUT



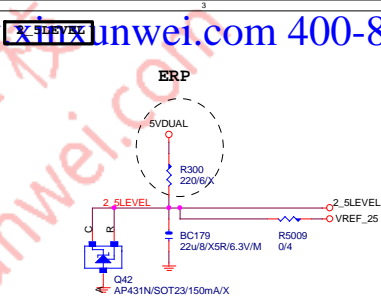
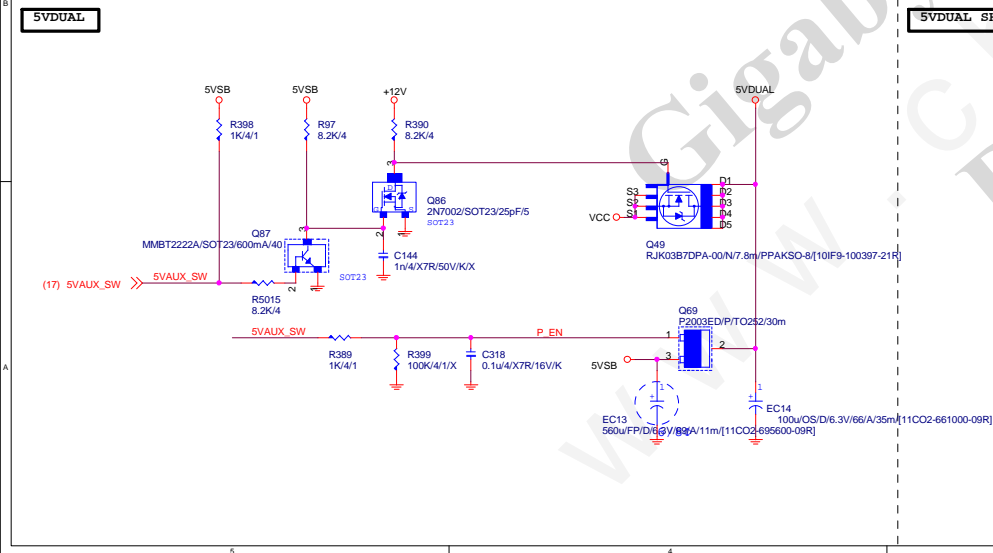
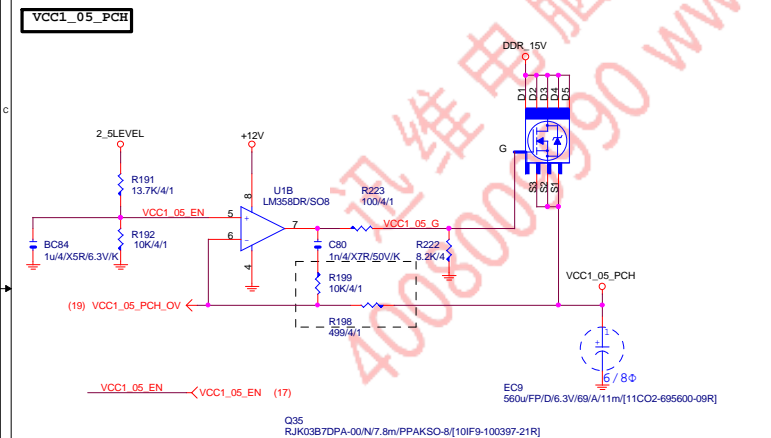
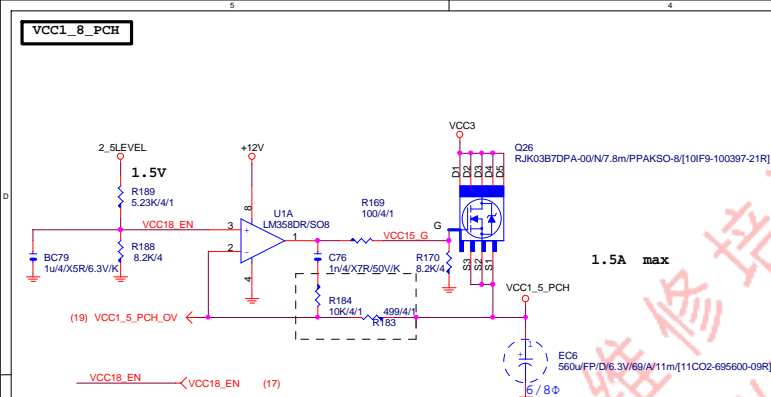
AZALIA FRONT PANEL



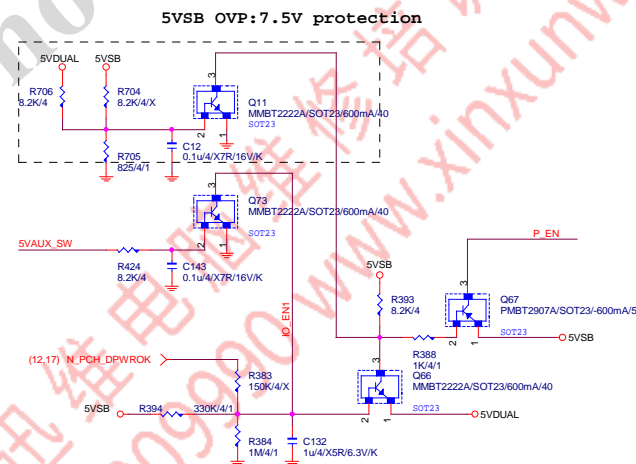
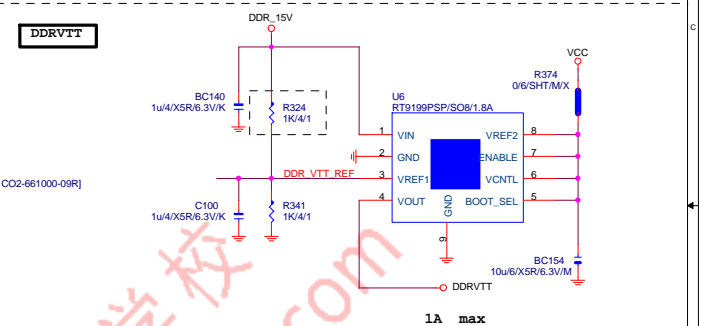
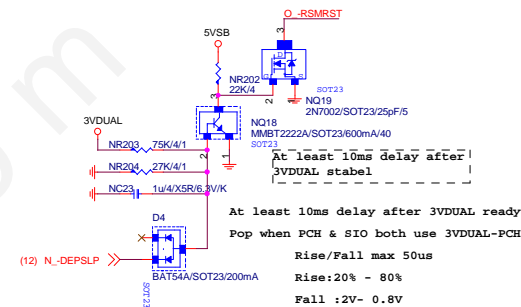
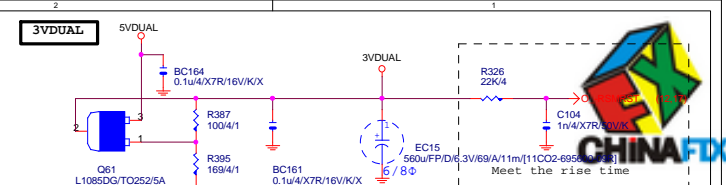
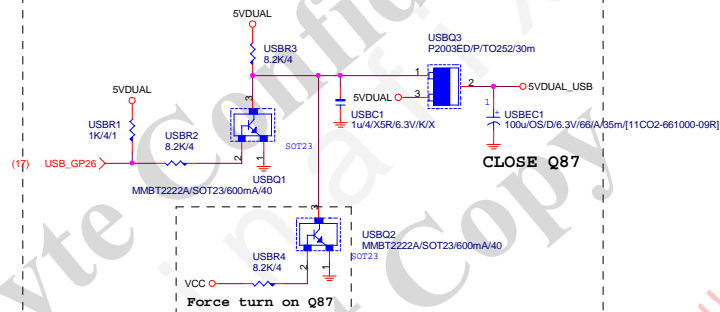
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5VDUAL_USB Ctrl	GPIO	5VDUAL_USB
KB_USB, R_USB30,	High	Power ON
USB_LAN_F_USB30,	Low	Power OFF
F_USB2 Power		





Pin 1 to 12 connection diagram for the APW212BK/V/SN/2SH-K/PA66 BLACK CONNECTOR. The diagram shows a 12-pin connector with pins numbered 1 to 12. Pin 1 is connected to VCC3. Pin 2 is connected to VCC3. Pin 3 is connected to VCC3. Pin 4 is connected to VCC3. Pin 5 is connected to VCC3. Pin 6 is connected to VCC3. Pin 7 is connected to VCC3. Pin 8 is connected to VCC3. Pin 9 is connected to VCC3. Pin 10 is connected to VCC3. Pin 11 is connected to VCC3. Pin 12 is connected to VCC3. The connector is labeled with the following pin numbers and functions: 13: 3.3V, 14: -12V, 15: GND, 16: PSON, 17: GND, 18: GND, 19: GND, 20: -5V, 21: 5V, 22: 5V, 23: 5V, 24: 3.3V. The connector is also labeled with the following functions: 1: 3.3V, 2: 3.3V, 3: GND, 4: 5V, 5: GND, 6: 5V, 7: GND, 8: POK, 9: 5VSB, 10: 12V, 11: 12V, 12: 3.3V.

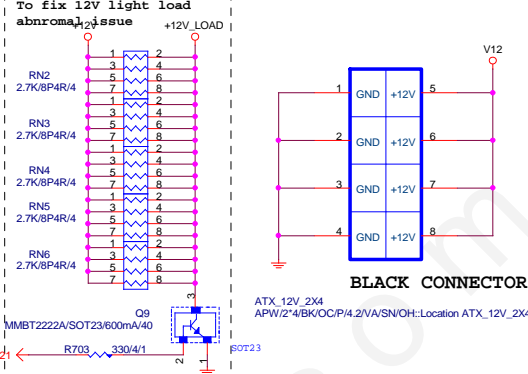
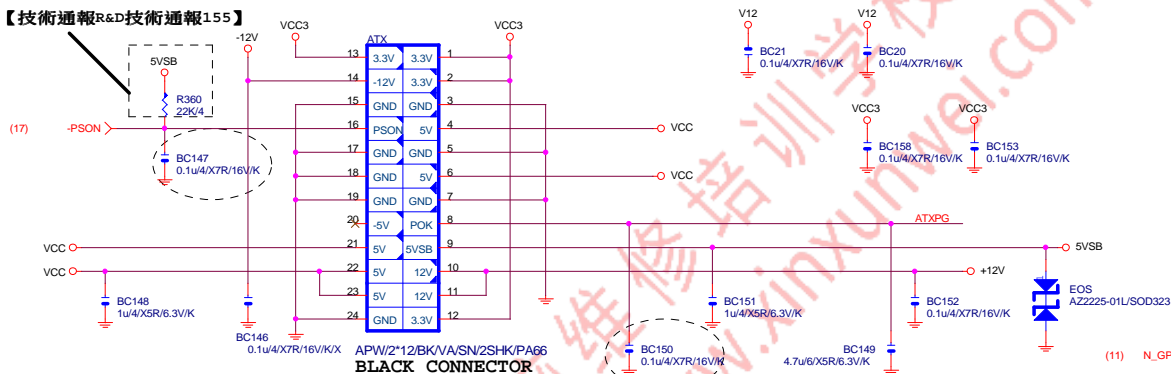
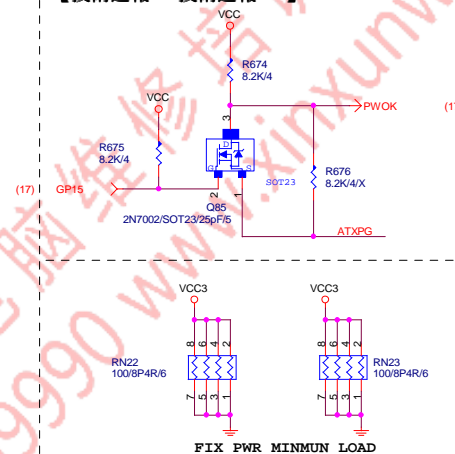


Figure 1: PCB layout of the 5VSB power plane. The layout shows a central 5VSB pad with a circular pattern of vias. Surrounding this are various components and pads labeled MH1 through MH6, AGND1, and K1 through K6. The layout is divided into two main sections: a top section with components MH1, MH2, MH3, AGND1, and a bottom section with components MH4, MH5, MH6. The central pad is labeled 'HOLE_3/X' and 'HOLE_4-RH-1'. The bottom section also includes a 'HOLE_3/X' label. The layout is designed to ensure proper power distribution and grounding for the 5VSB rail.

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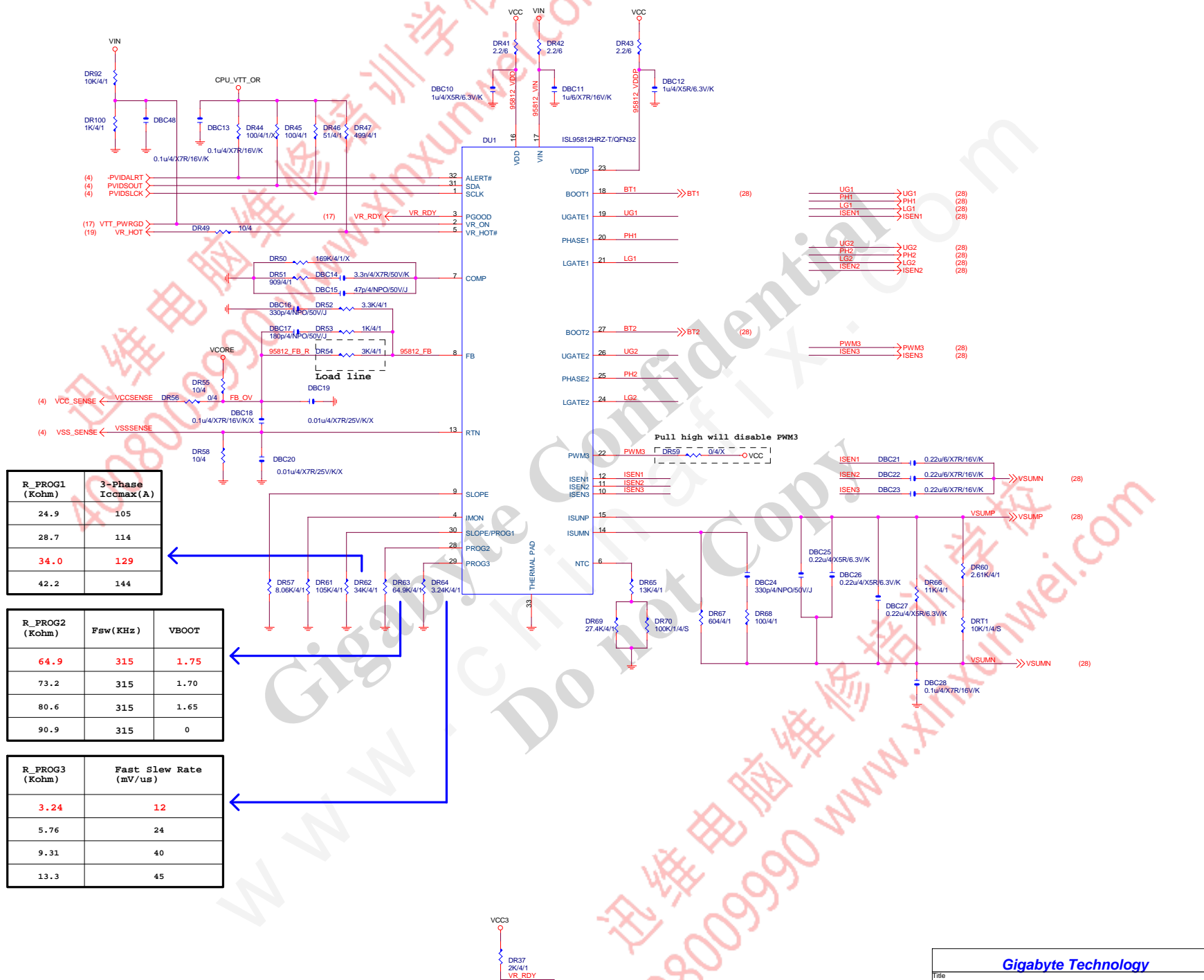


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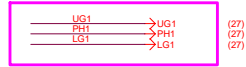
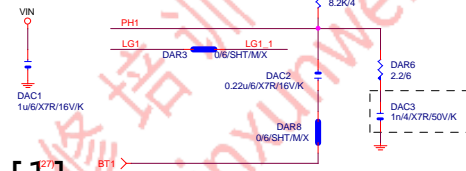
ATX CONNECTOR

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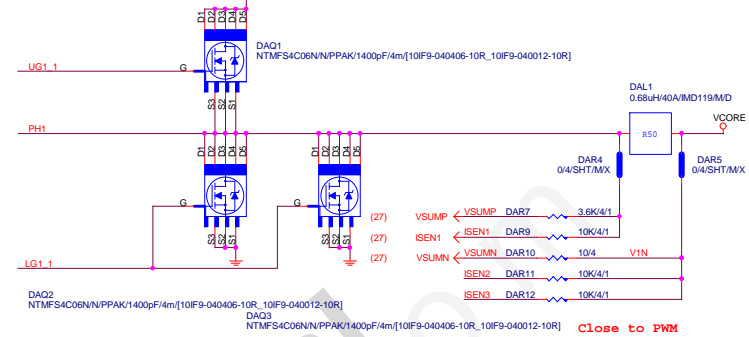
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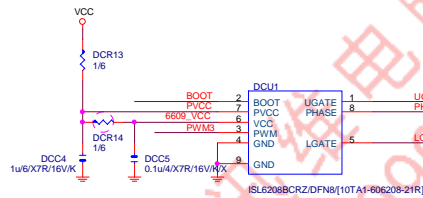
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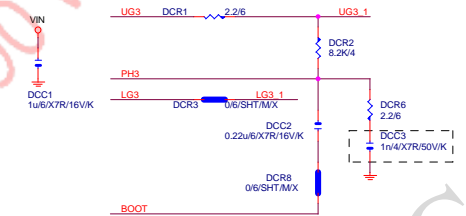
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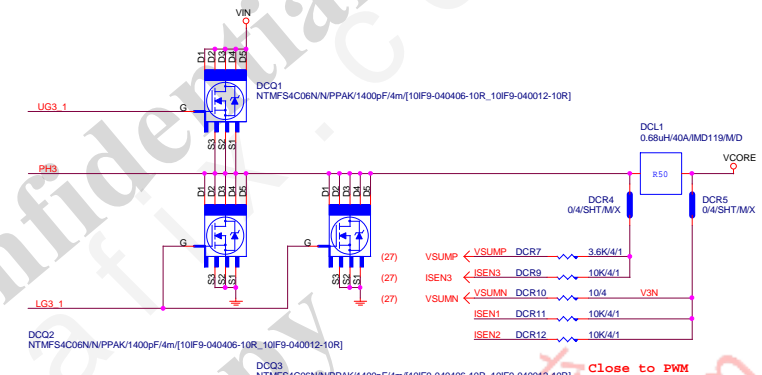
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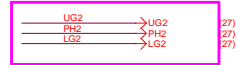
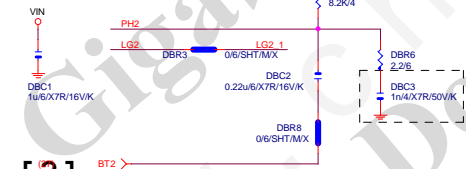
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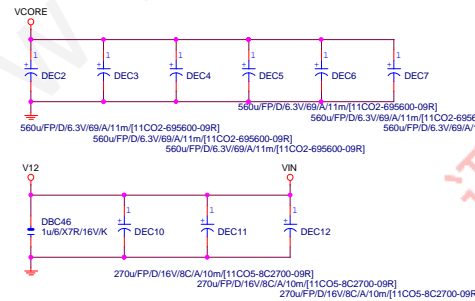
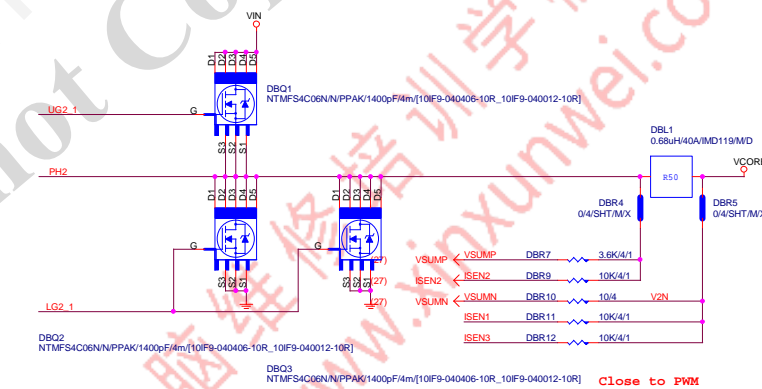
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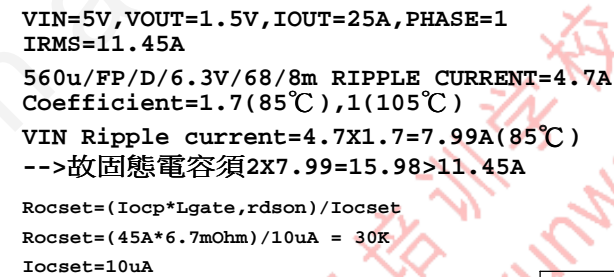
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